	Application No.	Applicant(s)
Notice of Allowability	10,507.001	
	10/707,961 Examiner	BONNEAU ET AL. Art Unit
		Artom
	Esaw T. Abraham	2133
The MAILING DATE of this communication app All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85 NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT F of the Office or upon petition by the applicant. See 37 CFR 1.31	S (OR REMAINS) CLOSED in this a i) or other appropriate communication RIGHTS. This application is subject	pplication. If not included on will be mailed in due course. THIS
1. \boxtimes This communication is responsive to <u>09/11/06</u> .		
2. ☑ The allowed claim(s) is/are <u>1-8</u> .		
 Acknowledgment is made of a claim for foreign priority to a) All b) Some* c) None of the: 1. Certified copies of the priority documents have 2. Certified copies of the priority documents have 3. Copies of the certified copies of the priority documents have international Bureau (PCT Rule 17.2(a)). * Certified copies not received:	ve been received. ve been received in Application No.	
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDON! THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		y complying with the requirements
 A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which given 		
5. CORRECTED DRAWINGS (as "replacement sheets") mu	ust be submitted.	
(a) I including changes required by the Notice of Draftsper	rson's Patent Drawing Review (PTC	0-948) attached
1) 🗌 hereto or 2) 🔲 to Paper No./Mail Date	<u>.</u>	
(b) including changes required by the attached Examiner Paper No./Mail Date	r's Amendment / Comment or in the	Office action of
Identifying indicia such as the application number (see 37 CFR each sheet. Replacement sheet(s) should be labeled as such in	1.84(c)) should be written on the draw the header according to 37 CFR 1.12	rings in the front (not the back) of I(d).
 DEPOSIT OF and/or INFORMATION about the deposit attached Examiner's comment regarding REQUIREMENT 		
Attachment(s) 1. ☐ Notice of References Cited (PTO-892)	E Nation of later 1	Detent Application
 Induce of References Cited (FTO-692) Induce of Draftperson's Patent Drawing Review (PTO-948) 	5. Notice of Informal	
	6. ⊠ Interview Summar Paper No./Mail D	
 Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 	7. Examiner's Amend	dment/Comment
4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	8. Examiner's Statem	nent of Reasons for Allowance
-	9. 🗌 Other)
		DVI AMADOE
		JY LAMARRE ARY EXAMINER
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EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and or additions be acceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no latter than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Anthony J. Canale on 09/14/06.

2. The application has been amended as follows:

As per claim 1:

Line, 6 please replace the phrase "a deserializer circuit" with ---a deserializer (DES) circuit---

Line, 6 please replace the phrase "to generate" with ---to output---.

Line, 9 please replace the phrase "a serializer circuit" with ---a serializer (SER) circuit---

Lines 10 and 11 please replace the phrase "an external clock" with ---a serializer clock---

As per claim 7:

Line 1 please replace the phrase "the external clock" with ---the serializer clock---

Examiner's statement for reason for allowance

3. Claims **1-8** have been allowed.

The following is an examiner's statement for allowance:

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As per claim 1:

The prior art, Payne (U.S. PN: 6,865,222) of record teach an integrated circuit (12) includes a phase locked loop (PLL) (31), a serializer circuit (32) of known configuration, and a built-in self test (BIST) circuit (33) whereby the inputs to the integrated circuit (12) include a reference clock input receives a reference clock signal and further the inputs to the integrated circuit (36) further include a parallel data input (37) which accepts 7-bit words, and a built-in self test circuit enable (BISTEN) signal input (38) (see col. 3, lines 31-40 and abstract). The prior art, Ramamurthy et al. (U.S. PN: 5,790,563) of record teach an integrated circuit 10 has a transmitter (12) and a receiver (14), a serializer 16 associated with the transmitter (12) and a deserializer (18) associated with the receiver (14). The serializer provides specialized functions for converting incoming data from several data streams (as from a parallel input or several serial inputs) into a single serial output. The deserializer (16) separates a single serial input (22) into divergent outputs. Further, Ramamurthy teach a pattern generator (24) provides a (20) bit output through a pattern generator output signal path (26) to a multiplexor (28). However, the prior arts taken singly or in combination fail to teach. anticipate, suggest, or render obvious a serializer/deserializer (SERDES) circuit having built-in self-test (BIST) capabilities that is configured to perform jitter sensitivity characterization, comprising a clock and data recovery (CDR) circuit coupled to said SERDES circuit that generates recovered clock and data from an incoming serial data stream, a deserializer circuit (DES) connected to said CDR circuit to output corresponding data (Parallel Data Out) and clock (DES clock) in a programmable

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pattern generator generating BIST patterns; a serializer circuit that receives either the a parallel format, BIST patterns or the input data (Parallel Data In) in a parallel format on a data input of the serializer circuit and a serializer clock (SER clock) on a clock input of the serializer circuit to generate a serial data stream, a delay perturbation circuit for adding a perturbation delay to said serial data stream to produce a perturbed serial data stream; a multiplexor circuit to output either the serial data stream or the perturbed serial data stream in a loop back to the CDR circuit; a control logic circuit block coupled to said deserializer circuit to detect a start-of-frame pattern using a dedicated signal (FD) and coupled to the programmable pattern generator and the perturbation circuit. Consequently, claim 1 is allowed over the prior art.

Claims 2-8, which is/are directly or indirectly dependent/s of claim 1 are also allowable over the prior art of record.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 5,790,563 Ramamurthy et al.

US PN: 6,865,222 Payne

US PN: 6,215,835 Kyles

US PN: 6,658,363 Mejia et al.

US PN: 6,725,408 Cao et al.

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Any inquiry concerning this communication or earlier communication from the

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examiner should be directed to Esaw Abraham whose telephone number is (571) 272-

3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's

supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers

for the organization where this application or proceeding is assigned are (571) 273-8300

for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for published

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questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

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GUY LAMARRE PRIMARY EXAMINER